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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/476,862	01/03/2000	AKIRA TSUKIHASHI	005586-20026	8395

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EXAMINER	
PATEL, GAUTAM	
ART UNIT	PAPER NUMBER
2653	7

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/476,862	Applicant(s) Tsukihashi
	Examiner Gautam R. Patel	Art Unit 2653

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *three* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Jan 18, 2002*

2a) ☒ This action is **FINAL.** 2b) ☐ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-12* is/are pending in the applica

4a) Of the above, claim(s) _____ is/are withdrawn from considera

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1-12* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirem

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15) ☒ Notice of References Cited (PTO-892)

16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

17) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____

18) ☐ Interview Summary (PTO-413) Paper No(s). _____

19) ☐ Notice of Informal Patent Application (PTO-152)

20) ☐ Other:

Response to Amendment

1. This is in response to amendment filed on 1-18-02 (Paper # 6).

2. Claims 1-12 remain for examination.

Claim Rejections - 35 U.S.C. § 103

3. The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
>
> Subject matter developed by another person, which qualifies as prior art only under subsection (f) or (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

4. Claims 1-12 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Shinada et al., US. patent 5,436,875 (hereafter Shinada) in view of Landry et al., US. patent 5,434,997 (hereafter Landry).

As to claim 1, Shinada discloses the invention as claimed [see Figs. 1-16] including a buffer memory, a data processing circuit and a system control circuit, comprising:

a. a buffer memory fig. 1, units 18 and 22] for temporarily storing the received data [col. 6, lines 1-5];

b. a data processing circuit [fig. 1, units 14 and 6] for preparing the recording data to record onto the disk, based on the received data read from the buffer memory [col. 6, lines 54-59; and

c. a system control circuit [fig. 1, unit 10] for controlling writing and reading of the received data with respect to the buffer memory, and operation of the data processing circuit [col. 5, lines 40-42 and col. 5, lines 65-68], wherein the system control circuit suspends operation of the data processing circuit until an amount of received data equivalent to a predetermined writing capacity has been stored in the buffer memory, and releases suspension of the operation of the data processing circuit when an amount of received data equivalent to the predetermined writing capacity has been stored in the buffer memory [col. 8, lines 19-55];

Shinada discloses all of the above elements including system control circuit for suspending the operation of the data processing circuit. Shinada does not specifically disclose well known methods of suspending this operation and details of the suspension circuit to the extent claimed. However Landry clearly discloses:

data processing circuit for recording data being placed in a suspended state by interrupting the power sully or by halting the supply of an operation clock [col. 2, lines 19-40 and col. 16, lines 13-61; Landry]. Both Shinada and Landry are interested in controlling the recording operation of the dat and avoid wrong data recording by checking the data content against some reference [such as threshold] and controlling the recording operation. It would have been obvious to one of ordinary skill in the at the time of invention to have provided the system of Shinada with details of controlling the data recording by halting the system clock in the system of Shinada, because doing so would have provided a mechanism for localizing the error on the spot and correct it [see col. 1, lines 13-52; Landry].

5. As to claim 2, Shinada discloses:

a writing circuit [fig. 1, unit 4] for writing the recorded data supplied from the data processing circuit, onto the disk, wherein the system control circuit stores an address successive to an address of received data last recorded onto the disk, as a recording start address on the disk, and controls the writing circuit so as to write the recording

data supplied from the data processing circuit onto the disk at the recording start address [col. 5, lines 60-64 and col. 12, lines 48-60].

6. As to claim 3, Shinada discloses:

the system control circuit synchronizes the recording data to be newly recorded onto the disk, supplied from the data processing circuit to the writing circuit, with recording data recorded on the disk [col. 6, lines 12-28], said data processing circuit being operated in synchronism with a reproduction clock obtained by reproducing the data already recorded on the disk [col. 8, line 57 to col. 9, line 33].

7. As to claim 6, Shinada discloses:

the writing capacity of the buffer memory is set at full memory capacity of the buffer memory deducted by an amount of data expected to be written into the buffer memory before data recording onto the disk is resumed [col. 6, lines 16-23].

8. As to claim 7, it is rejected for the same reasons set forth in the rejection of claims 1 and 2, supra.

9. As to claims 8-9, they are rejected for the same reasons set forth in the rejection of claims 2-3, supra.

10. As to claim 12, it is rejected for the same reasons set forth in the rejection of claim 6, supra.

11. As to claim 4, Shinada discloses:

a motor control circuit [fig. 1, unit 7] for controlling a motor for driving the disk, wherein the motor control circuit controls the motor such that the disk rotates, while operation of the data processing circuit is suspended [col. 5, line 40 to col. 6, line 40];

Shinada does not specifically discloses that speed of the disk before and after the suspension of the data recording is same. "Official Notice" is taken that both the concept and the advantages of providing a constant speed before and after the suspension of data recording are well known. It would have been obvious to provide a constant speed to Shinada's system as this constant speed is known to provide the system with less amount of control so as not to vary the speed while data is buffered thus reducing power consumption and control circuitry to vary the speed. These concepts are well known in the art and do not constitute a patentably distinct limitation, per se [M.P.E.P. 2144.03].

12. As to claim 5 Shinada does not specifically discloses that the buffer memory is set at a full memory capacity. "Official Notice" is taken that both the concept and the advantages of setting the buffer memory capacity at full capacity are well known in the art. It would have been obvious to provide a full capacity to buffer memory in Shinada's system as this setting the capacity to full allows the system to use the full capability of the buffer. Since real estate in the integrated circuits and on the board are at premium one of ordinary skill in the art would have been able to provide the mechanism to use full capability of the buffer so as not to waste premium space in the buffer. These concepts are well known in the art and do not constitute a patentably distinct limitation, per se [M.P.E.P. 2144.03].

13. As to claim 10, it is rejected for the same reasons set forth in the rejection of claim 4, supra.

14. As to claim 11, it is rejected for the same reasons set forth in the rejection of claim 5, supra.

Other prior art cited

15. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

    a. Ishibashi et al. (US. patent 5,354,975) "Contectless data processing apparatus".

    b. Tsuboi et al. (US. patent 5,307,473) "Controller for storage unit and method of controlling storage unit".

16. Applicant's arguments with respect to claims 1-12 have been considered but are deemed to be moot in view of the new grounds of rejection.

17. Applicant's amendment necessitated the new grounds of rejection presented in this office action. Accordingly, **THIS ACTION IS MADE FINAL**. See M.P.E.P. § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 C.F.R. § 1.136(a).

Contact information

18. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gautam R. Patel whose telephone number is (703) 308-7940. The examiner can normally be reached on Monday through Thursday from 7:30 to 6.

The appropriate fax number for the organization (Group 2650) where this application or proceeding is assigned is (703) 872-9314.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. William Korzuch, can be reached on (703) 305-6137.

Any inquiry of a general nature or relating to the status of this application should be directed to the group receptionist whose telephone number is (703) 305-4700 or the group Customer Service section whose telephone number is (703) 306-0377.

GRP

Gautam R. Patel
Patent Examiner
Group Art Unit 2653

February 24, 2002

W. R. YOUNG
PRIMARY EXAMINER